

The Examiner rejected claims 1-3, 5, 7-22, 29-31, 33, and 35-50 as being anticipated by Woo et al. (U.S. Patent No. 6,067 and 140). The rejection of claims 1-3, 5, and 7-22 is respectfully traversed and reconsideration is requested.

Claims 1-3, 5, 7-22, 29-31, 33, and 35-50 are allowable over the cited references in that each of these claims recites a combination of elements including, for example, an electric field inducing window and a photo-alignment layer having a pre-tilt angle on at least one of the first and second substrates. The cited reference, Woo et al., fails to disclose at least these features of the claimed invention. In particular, Woo et al. does not teach or suggest an electric field inducing window.

In Woo et al., the metal layer 130 is formed by etching a metal layer such as Ta, Al, and Al alloy film so that the metal layer 130 functions as an electrode for the storage capacitor and also as a shielding layer like a black matrix layer (see column 3, lines 12-16). As recited by independent claim 1, the electric field inducing window is in the pixel region. As recited by claim 29, the electric field inducing window is in the pixel electrode. The mere etching of a metal layer does not teach or suggest an electric field inducing window as recited by the claims.

The Examiner stated, on page 2 of the final Office Action, that "*Applicants do not clearly define the term 'electric field inducing window'*" and therefore, the Examiner has given the term its "*broadest reasonable interpretation.*" However, Applicants have clearly described the term "electric field inducing window" for example, and not by way of limitation, at least on pages 9, 11, and 12 of the specification and the feature is shown in all of the figures. The Applicant is his own lexicographer, and terms in the claims should be examined accordingly and not given a meaning by the Examiner.

Accordingly, Applicants respectfully submit that independent claims 1 and 29, and claims 2-3, 5, 7-22, 30, 31, 33, and 35-50 which depend therefrom, are allowable over the cited references.

The Examiner rejected claims 27 and 28, which depend from claim 1, and claims 55 and 56, which depend from claim 29, under 35 U.S.C. § 103(a) as being unpatentable over Woo et al.

Applicants respectfully note that, as discussed above with regard to independent claims 1 and 29, Woo et al. fails to disclose at least electric field inducing window and a photo-alignment layer having a pre-tilt angle on at least one of the first and second substrates, as recited in claims 1 and 29. Thus, Applicants submit that the features recited by claims 27 and 28, 55, and 56 could not have been obvious to one of skill in the art in view of Woo et al., as Woo et al. fails to teach, *inter alia*, at least an electric field inducing window and a photo-alignment layer having a pre-tilt angle on at least one of the first and second substrates.

The Examiner rejected claims 4, 23-26, 32, and 51-54 under 35 U.S.C. § 103(a) as being unpatentable over Woo et al. in view of Bos et al. (U.S. Patent No. 6,141,074).

Specifically, the Examiner states “*the term ‘reverse rubbing’ treatment in the Bos et al includes [sic] the method of forming the alignment by rubbing (col. 8., ln. 1-12). In addition, Bos et al. do disclose the alternative method to form an alignment layer having a small pretilt angle by using photolithography (i.e, using UV light)(col.15, lines 1-5).*”

Applicants respectfully submit that Bos et al. does not cure the deficiencies in Woo et al., as discussed above. Specifically, claims 4, 23-26, 32, and 51-54 are allowable over the cited references in that each of these claims recites a combination of elements including, for example, an electric field inducing window and a photo-alignment layer having a pre-tilt angle on at least one of the first and second substrates. The cited primary reference, Woo et al., fails to disclose at least these features of the claimed invention. Therefore, Applicants

respectfully submit that claims 4, 23-26, 32, and 51-54 are allowable over the cited references.

The Examiner rejected claims 6 and 34 under 35 U.S.C. § 103(a) as being unpatentable over Woo et al. in view of the article by Koma et al. entitled, "No-Rub Multi-Domain TFT Using Surrounding-Electrode Method."

As discussed above with regard to claims 1 and 29, the primary reference Woo et al. fails to disclose an electric field inducing window and a photo-alignment layer having a pre-tilt angle on at least one of the first and second substrates, and by virtue of their dependency on claims 1 and 29, respectively, claims 6 and 34. Koma et al. does not teach or suggest these features of the claimed invention. Applicants submit that the combination of Woo et al. and Koma et al. do not teach or suggest these features. Accordingly, Applicants respectfully submit that claims 6 and 34 are allowable over the cited references.

Applicants believe the foregoing remarks place the application in condition for allowance and early, favorable action is respectfully solicited.

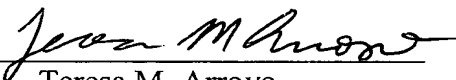
If the Examiner deems that a telephone call would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 624-1200. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete

the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911.

Respectfully submitted,

LONG, ALDRIDGE & NORMAN, LLP

By: 
Teresa M. Arroyo
Registration No.: 50,015

701 Pennsylvania Avenue, N.W.
Sixth Floor, Suite 600
Washington, D.C. 20004
(202) 624-1200
Date: February 6, 2002

MARKED UP VERSION OF AMENDED SPECIFICATION PARAGRAPHS:

Page 2, Paragraph beginning at Line 23:

The conventional rubbing method has been widely used as a [mean] means for applying an uniaxial extension process on a liquid crystal alignment layer so as to obtain a wide area and a high speed process and to simplify the manufacturing processes. Rubbing a substrate coated with polymer with a cloth is a simple method.

Page 6, Paragraph beginning at Line 5:

Fig. 2 is a [plane] plan view showing a multi-domain liquid crystal display device according to the present invention.

Page 6, Paragraph beginning at Line 11:

Figs. 5A, 5B, 5C, 5D and 5E are [plane] plan views showing first embodiments of the present invention.

Page 6, Paragraph beginning at Line 13:

Figs. 6A, 6B, 6C and 6D are [plane] plan views showing second embodiments of the present invention.

Page 6, Paragraph beginning at Line 15:

Figs. 7A, 7B, 7C and 7D are [plane] plan views showing third embodiments of the present invention.

Page 6, Paragraph beginning at Line 17:

Figs. 8A and 8B are [plane] plan views showing fourth embodiments of the present invention.

Page 6, Paragraph beginning at Line 26:

Figs. 1A, 1B and 1C are sectional views of the multi-domain liquid crystal display device of the present invention. Fig. 2 is a [plane] plan view showing of the multi-domain liquid crystal display devices of the present invention, and Fig. 3 and Fig. 4 are sectional views showing the view along lines A-A' and B-B' respectively of Fig. 2.

Page 7 and Paragraph beginning at Line 1:

As shown in the figures, the multi-domain liquid crystal display device according to the present invention comprises first and second substrates, a plurality of gate bus lines 1 arranged in a first direction on the first substrate, and a plurality of data bus lines 3 arranged in a second direction on the first substrate to define a pixel region. A TFT is formed on each pixel region of the first substrate 31 and comprises a gate electrode 11, a gate insulator 35, a semiconductor layer 5, an ohmic contact layer 6, source[/] and drain electrodes 7[,] and 9, etc. A passivation layer 37 is preferably formed on the whole first substrate 31. A pixel electrode 13 is connected to the drain electrode 9. An electric field inducing window 51 is formed therein for the passivation layer 37.

Page 7 and Paragraph beginning at Line 27:

To manufacture the multi-domain LCD of the present invention, in each pixel region on the first substrate 31, a TFT is formed comprising a gate electrode 11, a gate insulator 35, a semiconductor layer 5, a ohmic contact layer 6 and source[/] and drain electrodes 7[,] and 9.

A plurality of gate bus lines 1 and a plurality of data bus lines 3 are formed to divide the first substrate 31 into a plurality of pixel regions.

Page 8, Paragraph beginning at Line 3:

The gate electrode 11 and the gate bus line 1 are formed by sputtering and patterning a metal such as Al, Mo, Cr, Ta, Al alloy, or an alloy of the combination of these metals, etc. The gate insulator 35 is formed by depositing SiN_x or SiO_x thereon using a [PECVD] [(Plasma Enhancement Chemical Vapor Deposition)] (PECVD) method.

Page 8, Paragraph beginning at Line 9:

Subsequently, the semiconductor layer 5 and the ohmic contact layer 6 are formed by depositing by PECVD and patterning amorphous silicon (a-Si) and doped amorphous silicon (n⁺ a-Si), respectively. Also, the gate insulator, a-Si and n⁺ a-Si can be deposited by PECVD, continuously, and the a-Si and n⁺ a-Si is patterned to form the gate insulator 35, the semiconductor layer 5 and the ohmic contact layer 6. Data bus line 3 and source[/] and drain electrodes 7[,] and 9 are formed by sputtering and patterning a metal such as Al, Mo, Cr, Ta, Al alloy or an alloy of the combination of these metals, etc.

Page 8, Paragraph beginning at Line 19:

The passivation layer 37 is formed with [BCB] [(BenzoCycloButene)] (BCB), acrylic resin, polyimide based compound (for example Polyimide, Polyamide, Polyamic acid, etc.), SiN_x or SiO_x on the whole first substrate 31. And the pixel electrode 13 is formed by sputtering and patterning a metal such as [ITO] [(indium tin oxide)] (ITO). The pixel electrode 13 is electrically connected with the source[/] and drain electrode 7[,] and 9 of the TFT through a contact hole 39.